(54) Title: METHOD FOR DEPOSITING A SELECTED THICKNESS OF AN INTERLEVEL DIELECTRIC MATERIAL TO ACHIEVE OPTIMUM GLOBAL PLANARITY ON A SEMICONDUCTOR WAFER
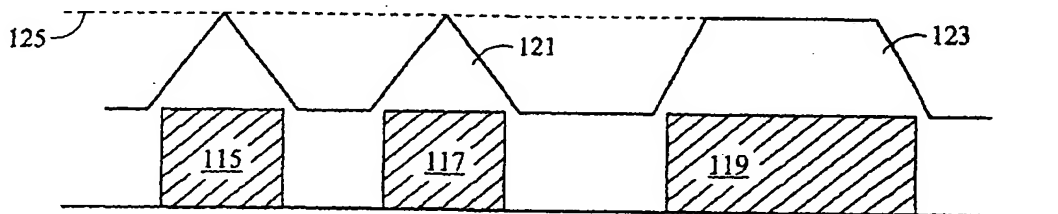
(57) Abstract: A method of depositing an interlevel dielectric material on a semiconductor wafer at a selected thickness such that the best global planarity of the dielectric layer is achieved. A model for the deposition of a silicon dioxide layer is developed based upon the physics of deposition and sputtering and based upon the minimum geometry of features in the semiconductor device. First the geometric parameters of the metal features are determined. Then, based upon the most aggressive aspect ratio between metal lines, the deposition rate to sputter rate ratio is calculated. The film thickness for optimum global planarity is determined based on the calculated ratio. The dielectric material (121, 123) is then deposited on the metal features (115, 117, 119) using HDP-CVD techniques in a manner using the calculated ratio to stop deposition at the determined film thickness such that the optimum thickness for global planarity is achieved.

METHOD FOR DEPOSITING A SELECTED THICKNESS
OF AN INTERLEVEL DIELECTRIC MATERIAL TO ACHIEVE
5   OPTIMUM GLOBAL PLANARITY ON A SEMICONDUCTOR WAFER

TECHNICAL FIELD

The present invention relates generally to the
field of silicon processing, and more specifically to a
10   method of forming an interlevel dielectric on a semicon-
ductor wafer.

BACKGROUND ART

In the construction of a semiconductor device,
15   many conductive device regions or layers are formed on a
semiconductor substrate. In order to isolate these lay-
ers or regions, an interlevel dielectric layer is formed
over these regions. Usually, a chemical vapor deposition
(CVD) technique is used to deposit the inter-level di-
20   electric layer over the conductive regions. In a chemi-
cal vapor deposition process, chemicals containing the
atoms or molecules required in the final film are mixed
and reacted in a deposition chamber to form a vapor. The
atoms or molecules deposit on the wafer surface and build
25   up to form a film. Common CVD methods include
atmosphere-pressure CVD (APCVD), low-pressure CVD (LPCVD)
and plasma-enhanced CVD (PECVD). The PECVD method pro-
vides an advantage over the APCVD and LPCVD methods in
that it can be carried out at lower substrate tempera-
30   tures. This is because the PECVD uses an rf-induced glow
discharge or plasma to transfer energy into the reactant
gases, rather than relying solely on thermal energy to
initiate and sustain chemical reactions. This allows
PECVD to be used to deposit films on substrates that do
35   not have the thermal stability to accept coating by other

methods, such as, for example, the formation of silicon nitride and silicon oxide over metals.

As advances are made in semiconductor technology, circuit elements and interconnections on wafers or

5 silicon substrates are becoming more and more dense. As the circuit densities continue to increase, the widths of insulator-filled gaps or trenches, provided to physically and electrically isolate circuit elements and conductive lines, decrease. This increases the gap aspect ratio,

10 which is usually defined as the gap height divided by the gap width. It is more difficult to fill these gaps with higher aspect ratios using the above CVD techniques, which can lead to unwanted voids and discontinuities in the insulating or gap-fill material.

15 Presently, high density plasma chemical vapor deposition (HDP-CVD) techniques are used to fill gaps having higher aspect ratios. HDP-CVD allows for the addition of a sputter component to the plasma deposition process which can be controlled to assist in gap-filling

20 during deposition processes in a manner superior to the other CVD methods noted above. Typical HDP deposition processes employ chemical vapor deposition with a gas mixture containing oxygen, silane, and inert gases, such as argon, to achieve simultaneous dielectric etching and

25 deposition. In an HDP process, an RF bias is applied to a wafer substrate in a reaction chamber. Some of these gas molecules, particularly argon, are ionized in the plasma and accelerate toward the wafer surface when the RF bias is applied to the substrate. Material is thereby

30 sputtered when the ions strike the surface. This results in the dielectric material deposited on the wafer surface being simultaneously sputter etched. This helps to keep gaps open during the deposition process, which allows gaps with higher aspect ratios to be filled.

The conductive elements and interconnections,
over which the interlevel dielectric is to be deposited,
typically comprises a plurality of metal features, some
of which have different sizes. A typical conductive
5   pattern comprises a dense array of metal features, typi-
cally separated by gaps having a width of less than about
one micron. However, a metal feature next to one of the
metal features of the dense array, may be considerably
larger than the metal features of the dense array. In
10   the case where an adjacent feature has an upper surface
area of a size greater than the upper surface area of the
metal features of the dense array, then when a gap-fill-
ing dielectric layer is deposited, a step is formed with
increasing height between the relatively smaller metal
15   feature of the dense array and the relatively larger
metal feature. With reference to Fig. 1, the metal fea-
tures 15 and 17 of a dense array 12 have an upper surface
area that is smaller than the upper surface area of a
much larger metal feature 19 that is located next to the
20   dense array 12. When a dielectric layer 21 is deposited
over the metal features 15, 17, 19, a step 27 is formed
between the thickness 23 of dielectric material required
to cover the smaller features 15, 17 and the thickness of
dielectric material 25 required to cover the feature with
25   the larger upper surface area. This step 27 makes it
extremely difficult to planarize the dielectric layer
that was deposited on the metal features. What is needed
is a way to deposit a dielectric layer that minimizes the
step height and improves the overall planarity of the
30   layer across the semiconductor wafer.

        It is the object of the present invention to
provide a method of depositing an interlevel dielectric
material on a semiconductor wafer that minimizes the
amount of step height between metal features.

It is a further object of the present invention to provide a method of depositing an interlevel dielectric material on a semiconductor wafer based on a theoretical prediction of the high density plasma chemical

5   vapor deposition thickness of the dielectric material that provides the best global planarity across the wafer and across each die.

SUMMARY OF THE INVENTION

10   The above objects have been achieved by a method of depositing an interlevel dielectric material on a semiconductor wafer at a selected thickness such that the best global planarity of the dielectric layer is achieved. A model for the deposition of a silicon diox-

15   ide dielectric layer is developed based upon the physics of deposition and sputtering, and based upon the minimum geometry of metal features in the semiconductor device. The HDP deposition model developed in this invention is then used to predict the optimum thickness of deposited

20   film that, after a conformal cap deposition and chemical mechanical polishing (CMP) planarization, provides the best global planarity across the wafer. First, the geometric parameters of the metal features, such as the minimum width, pitch and height, are determined. Then,

25   based upon the most aggressive aspect ratio between metal lines, the chemical vapor deposition rate to sputter rate ratio (D/S) is calculated. The optimum film thickness of the deposited oxide is determined based on the minimum width and space of the metal features, the height of the

30   features, the deposition rate to sputter rate ratio, the angle of maximum sputter yield and the level of planarity required by the process. The dielectric material is then deposited on the metal features using HDP-CVD techniques in a manner using the calculated ratio to stop the depo-

sition at the determined film thickness such that the
optimum thickness for global planarity is achieved.

BRIEF DESCRIPTION OF THE DRAWINGS

5   Fig. 1 is a cross-sectional view of the HDP-CVD
deposition of a dielectric material on a plurality of
metal traces as known in the prior art.
           Fig. 2 is a cross-sectional view of the HDP-CVD
deposition of several layers of a dielectric material on
10   a plurality of metal traces as known in the prior art.
           Fig. 3 is a graph showing a typical relation-
ship between the incidence angle of the sputtering gas
(Ar) and the sputtering rate of the target material
(quartz).
15   Fig. 4 is a cross-sectional view of metal
traces, each having a dielectric material deposited
thereon at different deposition rate to sputter rate
ratios.
           Fig. 5 is a cross-sectional view of metal
20   traces having a dielectric layer deposited thereon and
showing the various dimensions of the parameters used in
the present invention.
           Figs. 6A and 6B are graphs showing the rela-
tionship of step height versus HDP deposition thickness
25   for different deposition rate to sputter rate ratios.
           Fig. 7 is a cross-sectional view of the HDP-CVD
deposition of a dielectric material on a plurality of
metal traces using the method of the present invention.

30   BEST MODE FOR CARRYING OUT THE INVENTION
           With reference to Fig. 2, in a typical HDP-CVD
deposition process, as known in the prior art, the vari-
ous layers of a dielectric material, such as silicon
dioxide, or quartz (SiO_2), are deposited over the metal
35   traces. Fig. 2 shows the dielectric material 22 being

divided into ten layers A - J, layer A being the first
layer deposited over the metal traces 14, 16, 18, and
layer J being the final layer deposited. As shown, the
layers A - J of the dielectric material 22 accumulate on
5   top of the metal traces 14, 16, 18 in the form of a tri-
angular structure. This is because, although the argon
gas molecules are sputtered uniformly across the surface,
the sputtering rate is faster at the corners of the metal
traces due to the angle of incidence of the sputtering
10   gas at the corners.

With reference to Fig. 3, there is an incidence
angle of the sputtering gas relative to the sputtering
surface that provides the maximum sputtering rate yield.
That maximum sputtering angle can vary and is determined
15   by the particular HDP-CVD equipment that is employed. In
most systems, the incidence angle that produces the maxi-
mum sputtering yield ranges from 45 degrees to 60 de-
grees. Because the angle of incidence at the corners of
the metal traces is at or near the angle of maximum
20   yield, the sputtering rate at the corners of the metal
traces is faster than the sputtering rate on top of the
metal traces. This causes the substrate material to form
in the shape of a triangular structure, as shown in Fig.
2. In the graph 30 of Fig. 3, the incidence angle 32 of
25   the sputtering gas is plotted against the sputtering rate
34 of the deposited surface material. In the preferred
embodiment of the invention, as shown in Fig. 3, the
angle of maximum sputtering yield is 60 degrees. The
range of sputtering 36 for maximum sputtering yield is
30   shown to be between 45 degrees and 70 degrees. There-
fore, a maximum sputtering yield angle of 60 degrees is
used in the calculations of optimum film thickness used
in the preferred embodiment of the present invention.

Referring back to Fig. 2, metal trace 14 is
35   covered by triangular dielectric structure 24 consisting

of three layers A, B and C. Similarly, metal trace 16 is
covered by a triangular dielectric structure 26 consist-
ing of layers A, B and C. Metal trace 18 has a wider
upper surface so therefore the size of the completed

5   triangular dielectric structure 28 over metal trace 18 is
much larger and consists of layers A - H. Each dielec-
tric layer A - J of the dielectric material 22 fills in
the gaps between the metal traces and also deposits on
top of the metal traces 14, 16, 18 in such a way as to

10   form the triangular structures 24, 26 and 28. As can be
seen in Fig. 2, the metal trace 18 having the wider sur-
face area requires more dielectric layers in order to
completely cover the metal trace with the triangular
structure 28. For example, when layer D is applied, the

15   triangular structures 24 and 26 have already been formed
over metal traces 14 and 16 and the dielectric material
of layer D just fills in around and between the metal
traces 14 and 16. However, the layer D continues to pile
on top of metal trace 18 to form the triangular structure

20   28. As can be seen, as additional layers of dielectric
material are applied, a large height differential, or
step height, is created between the tops of triangular
structure 24 and 26 and the top of triangular structure
28.

25   With reference to Fig. 5, the first step in the
method of the present invention is to determine the set
of geometric parameters of a series of metal features on
the semiconductor wafer surface. Each metal trace 61 has
a width (w) 68 and a height (h) 69. The triangular

30   structure 63, which is the dielectric material directly
on top of the metal trace 61, has a thickness (t) 65 and
an angle of sputtering yield (Θ) 70.
              Referring to Fig. 4, an additional geometric
parameter that is relevant in determining the deposition
35   rate to sputter rate is the amount of corner growth (x)

56, 57, 58 of the substrate on the top corner of the
trace. The deposition rate to sputter rate ratio at
which there is zero corner growth will vary depending on
the parameters of the particular HDP-CVD apparatus em-
ployed. Once these parameters have been determined, the
next step is to calculate a ratio between the deposition
rate and the sputtering rate based on the set of geomet-
ric parameters. In Fig. 4, trace 41 is covered by a
triangular structure 48 having a thickness (t) 42 and an
angle Θ. The deposition rate to sputtering rate ratio of
the insulating material that forms structure 48 on trace
41 is the deposition rate to sputter rate ratio at which
there is zero corner growth. The corner growth rate 56
is equal to zero since the sides of the triangular struc-
ture 48 are aligned directly with the upper corner of the
metal trace 41. In the preferred embodiment of the in-
vention, the deposition rate to sputter rate ratio at
which zero corner growth is obtained is equal to 3.2. In
comparison, the triangular structure 49 formed by sub-
strate material deposited on trace 43 is deposited at a
higher deposition rate to sputter rate ratio such as, for
example, a ratio of 4.5. At a deposition rate to sputter
rate ratio of 4.5, the sides of the triangular structure
49 spread outward from the metal trace 43 such that there
is a corner growth distance (x) 57. Because of the cor-
ner growth distance (x) 57, the thickness 44 of the di-
electric layer required to form the triangular structure
49 is greater than the thickness 42 of the dielectric
layer required to form the triangular structure 48 on
trace 41. Additionally, as shown in Fig. 4, the triangu-
lar structure 50 formed by the dielectric layer deposited
on trace 45 is deposited at an even higher deposition
rate to sputter rate ratio, such as 7.5. With the higher
deposition rate to sputter rate ratio of 7.5, the trian-
gular structure 50 covering the metal trace 45 has an

even larger corner growth (x) 58 and a greater thickness
46 than the other metal traces 41 and 43 which have lower
deposition rate to sputter rate ratios. Therefore, it
can be seen that in order to get the lowest possible peak
5   on the triangular structures of dielectric material
formed over the metal traces, it is preferable to choose
a deposition rate to sputter rate ratio wherein the cor-
ner growth (x) is minimized.

However, the deposition rate to sputter rate
10   ratio should not be too low. If the deposition rate to
sputter rate ratio is lower than the ratio at which there
is zero corner growth, then the triangular structure does
not cover the entire upper surface of the metal trace 41
and the corners of the upper surface of the metal trace
15   41 will be sputtered away, which is not desirable.

In order to determine the film thickness (t) at
which the triangular structure is complete, the geometri-
cal relation between the height and width of the triangu-
lar structure for the metal trace having the smallest
20   width 61 is used. With reference to Fig. 5, the triangu-
lar structure 63 covering the smallest metal trace 61,
has a height or thickness (t) 65 and a base equal to the
width (w) 68 plus two times the corner growth (x) 76.
The triangular structure also has two sides, each having
25   a length (ℓ) 60. In the preferred embodiment of the
invention, wherein the angle of incidence Θ is equal to
60 degrees, all of the sides of the triangle have the
same length so that $\ell = 2x + w$. Using trigonomic rela-
tionships, $\sin \Theta = \dfrac{t}{\ell}$, which can be rewritten, $t = \sin \Theta$
30     $(w + 2x)$. Therefore, in the preferred embodiment of the
invention, the film thickness is equal to a value defined
by the width of the metal trace plus two times the corner
growth (the distance x on each side of the metal trace),
multiplied by the sine of the angle Θ which produces the
35   maximum sputtering yield. In the general case, in which

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the angle Θ is not equal to 60 degrees, the relationship
tan Θ = t/(½w + x) exists, so that t = tan Θ (½w + x).
Therefore, the film thickness is equal to a value defined
by one half of the width of the metal trace plus two
5   times the corner growth thickness multiplied by the tan-
gent of the angle Θ which produces the maximum sputtering
yield.

The deposition rate to sputter rate ratio (D/S)
is known in the art as being the effective thickness
10   deposited plus the sputter rate (SR), divided by the
sputter rate, or

$$D/S = \frac{eff. \ t + SR}{SR},$$

which can be rewritten as

15

$$D/S = \frac{eff. \ t}{SR} + 1$$

To determine the amount of corner growth (x), two scenar-
ios need to be considered. In the first case, the depo-
20   sition rate to sputter rate ratio is equal to the ratio
at which there is zero corner growth, D/S_0. In the second
case, the deposition rate to sputter rate ratio is equal
to the ratio at which the film thickness is to be deter-
mined, D/S. The deposition thickness is assumed to be
25   equal to the height of the metal feature, h. Using the
equation for D/S noted above results in, for the first
case:

$$D/S_0 = \frac{h}{SR_1} + 1,$$

30   and for the second case:

$$D/S = \frac{h}{SR_2} + 1.$$

These equations can be rearranged to produce the follow-
ing equations for the sputter rates,

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$$SR_1 = \frac{h}{(D/S_0 - 1)} \quad \text{and} \quad SR_2 = \frac{h}{(D/S - 1)}$$

The difference between the two sputtering rates (SR_1 – SR_2) is equivalent to the thickness of the corner growth,
x.   Therefore, the corner growth (x) can be defined as
the height of the metal trace, h, multiplied by the dif-
ference between one divided by the deposition rate to
sputter rate ratio at which there is zero corner growth
minus one and one divided by the deposition rate to sput-
ter rate ratio at which the optimum thickness is to be
determined minus one, or

$$x = h \left[\frac{1}{(D/S_0 - 1)} - \frac{1}{(D/S - 1)} \right]$$

The equation for corner growth relates the deposition
rate to sputter rate ratio to the optimum thickness of
the layers of dielectric material. The optimum film
thickness may be greater than or less than the height of
the metal feature, depending on the width of the feature,
w.

Referring to Fig. 5, two other values to be
defined are the local step height 66 and the global step
height 67.   The local step height 66 is the height be-
tween the top of the triangular structure covering the
trace and the height of the dielectric material located
outside the triangular structure. At the point where the
local step height is the greatest, the triangular struc-
ture formed on top of the trace is at a maximum and the
dielectric material located outside of the triangular
structure on the trace is at a minimum. As more dielec-
tric layers are added to the traces, the local step
height gets smaller as the dielectric material outside of
the triangular structure of the trace gets larger. The
global step height 67 is the difference between the top
of the triangular structure 63 covering the smallest

trace 61 and the top of the triangular structure 64 cov-
ering the largest trace 62. The global step height 67 is
smallest when the triangular structure 63 of the smaller
trace 61 reaches its peak. As more dielectric layers are
added and the triangular structure 64 of the larger trace
62 gets larger, the global step height 67 increases.

       With reference to Figs. 6A and 6B, the step
height is plotted versus the HDP deposition thickness of
the triangular structures. In Fig. 6A, the deposition
rate to sputtering rate ratio is 4. Graph 71 represents
the local step height and graph 81 represents the global
step height. As can be seen, as the thickness of the
dielectric material increases, the local step height 71
decreases, while the global step height 81 increases.
The point at which the global step height 81 starts to
increase and the local step height begins to decrease is
the point 91 of optimum thickness. In Fig. 6A the HTP
optimum thickness 91 is determined to be 0.5 µm. Fig. 6B
is the same graph except with a lower deposition rate to
sputtering rate of 3.5. In this case, the point where
the local step height 72 begins to decrease and the
global step height 82 begins to increase produces an
optimum thickness point 92 of 0.4 µm. Therefore, it is
clear that having a lower deposition rate to sputter rate
ratio, without going so low as to sputter the metal
trace, produces a minimum optimum thickness of the di-
electric layer.

       With reference to Fig. 7, once an optimum film
thickness has been determined based on the formulas de-
scribed above, the geometric parameters that are neces-
sary to achieve the optimum film thickness, such as the
gas flow rate, deposition rate, the amount of time needed
to deposition and sputter, plasma power, etc. are entered
into the machine that carries out the HDP-CVD process.
The HDP-CVD machine then applies the dielectric layer

over the traces in a manner as known in the art using the
parameters that were calculated to achieve the optimum
thickness of the dielectric layer. Optical measurement
tools are used to measure the film thickness. Ideally,
it is preferred that the thickness of the dielectric
layer deposited be equal to the determined film thick-
ness. Alternatively, the determined film thickness can
be just used as a guideline with allowable tolerances,
for example plus or minus twenty percent.

As shown in Fig. 7, when the optimum film
thickness of the dielectric layer is achieved, there is
little or no step height 125 between the height of the
dielectric layer 121 over the metal traces 115 and 117
and the height of the dielectric layer 123 over the
larger trace 119. By minimizing the step height, it
helps to make it easier to planarize the semiconductor
wafer. After the deposition of the insulating layer, a
conformal oxide cap is deposited on top of the dielectric
layer and then a chemical mechanical polishing step is
implemented to planarize the wafer. By applying the
dielectric material in a manner as described in the pres-
ent invention, step heights are reduced, which makes the
subsequent CMP steps easier to carry out, and addition-
ally provides better planarization of the oxide over the
metal traces.

Claims

1.   A method for depositing a selected thickness of a
dielectric material comprising:

5   determining a set of geometric parameters of a
series of metal features on a semiconductor wafer
surface,

                  calculating a ratio between a chemical vapor
deposition rate and a sputter rate based on the set of
10   geometric parameters for said wafer,

                  determining a film thickness based on the
calculated ratio, and

                  depositing the dielectric material on the metal
features in a manner using the calculated ratio to stop
15   deposition whereby an optimum thickness for global
planarity is achieved.

2.   The method of claim 1, wherein the set of geometric
20   parameters includes a minimum width, a minimum pitch and
a minimum height of the series of metal features.

3.   The method of claim 1, wherein the set of geometric
25   parameters includes a corner thickness of the dielectric
material at a top corner of one of the metal features.

4.   The method of claim 3, wherein the corner thickness
30   has a relationship to a minimum height of the metal
features multiplied by the difference between one divided
by the ratio of deposition rate to sputter rate at zero
corner growth minus one and one divided by the ratio of
deposition rate to sputter rate at a deposited thickness
35   minus one.

5.   The method of claim 4, wherein the determined film thickness has a relationship to a sine of an angle of maximum sputter yield multiplied by a value of twice the corner thickness plus the minimum width.

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6.   The method of claim 4, wherein the determined film thickness has a relationship to a tangent of an angle of maximum sputter yield multiplied by a value of one half of the minimum width plus the corner thickness.

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7.   The method of claim 1, wherein the dielectric material is deposited over the metal features at a thickness equal to the determined film thickness.

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8.   The method of claim 1, wherein the dielectric material is deposited over the metal features at a thickness that is within twenty percent of the determined film thickness.

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9.   The method of claim 1, further including the steps of:
            depositing a conformal cap oxide, and
            employing a chemical mechanical polishing technique to planarize the semiconductor wafer surface.

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10.   The method of claim 1, wherein the step of depositing the dielectric material on the metal features is carried out using a HDP-CVD process.
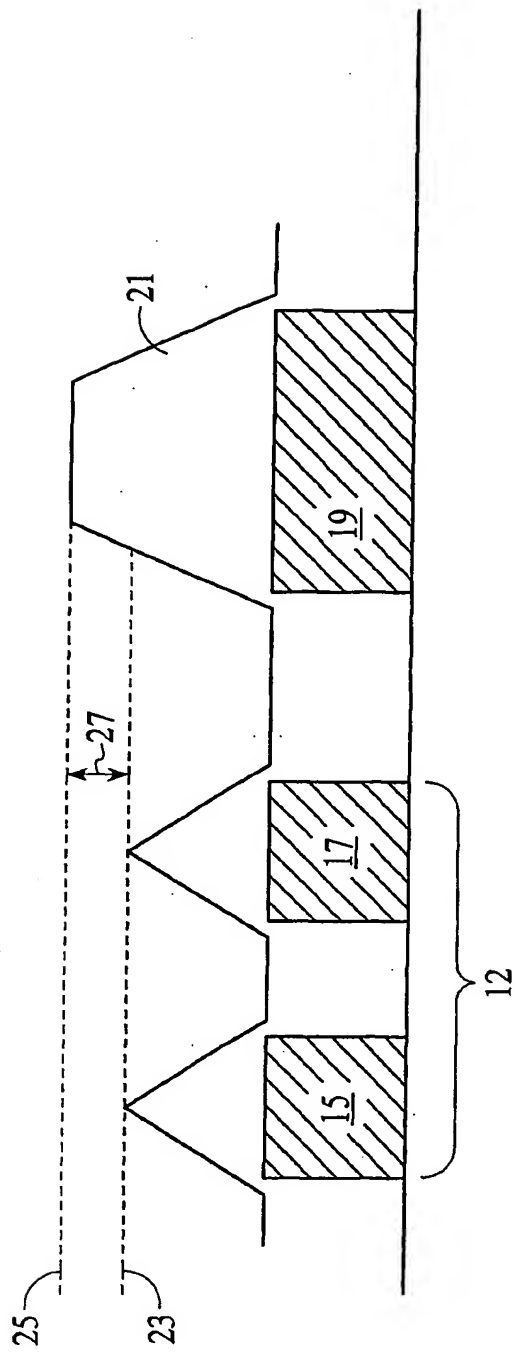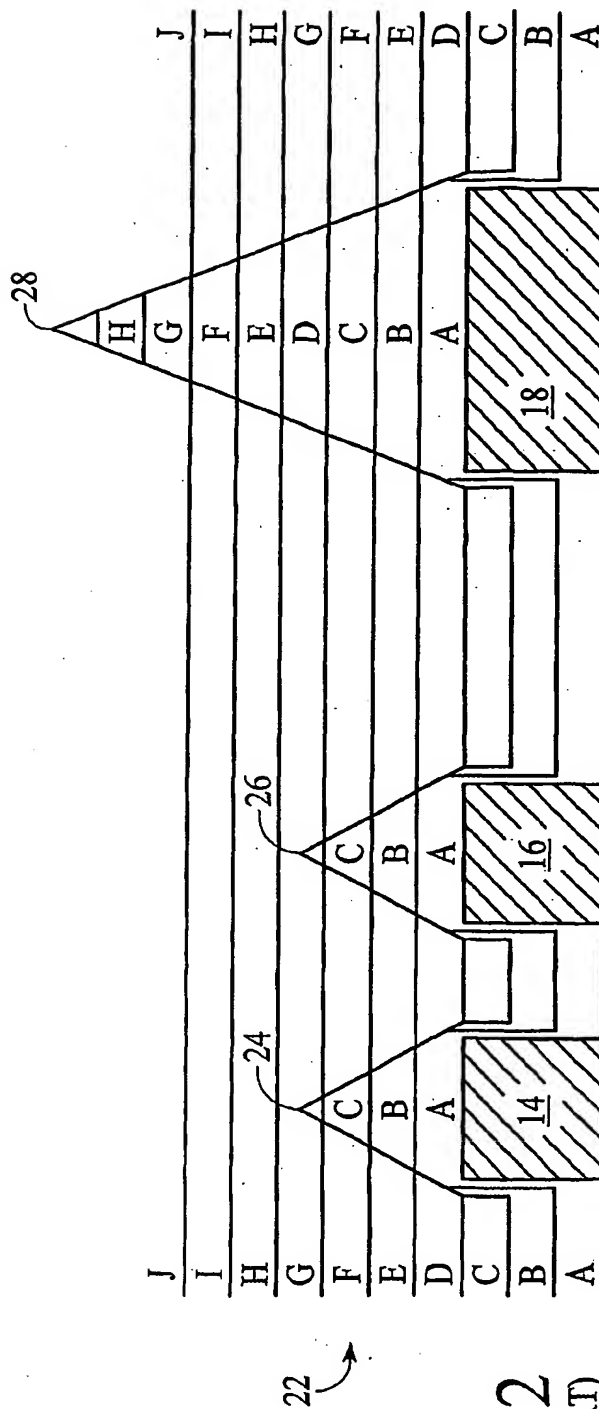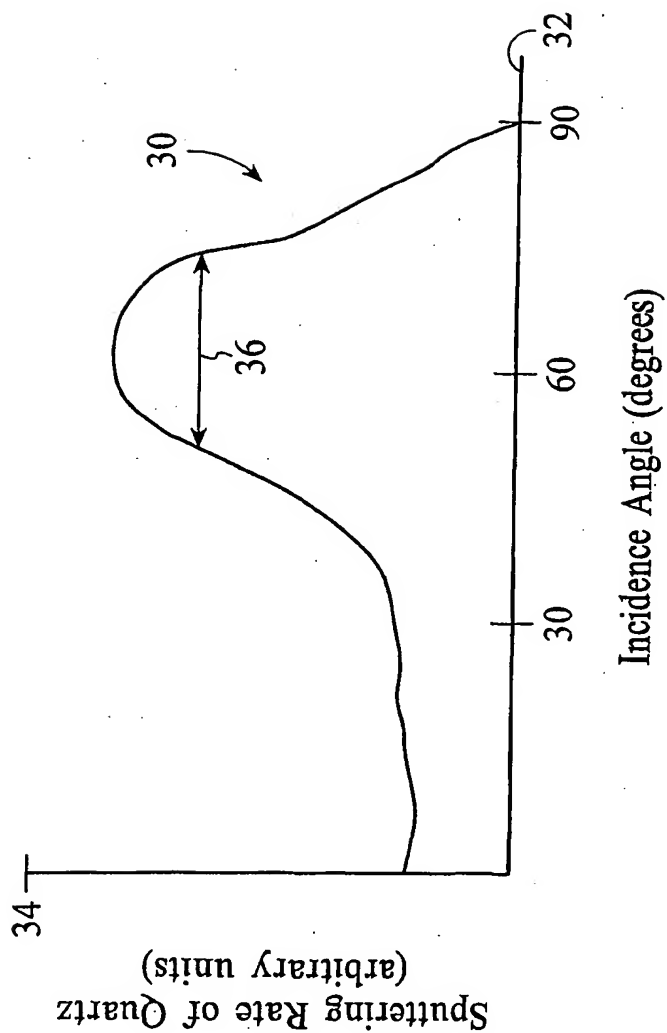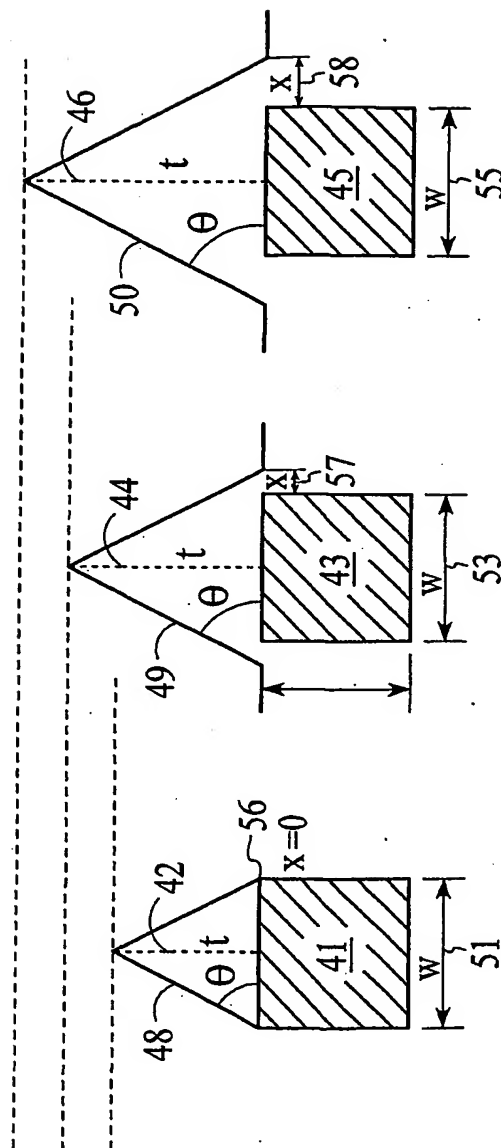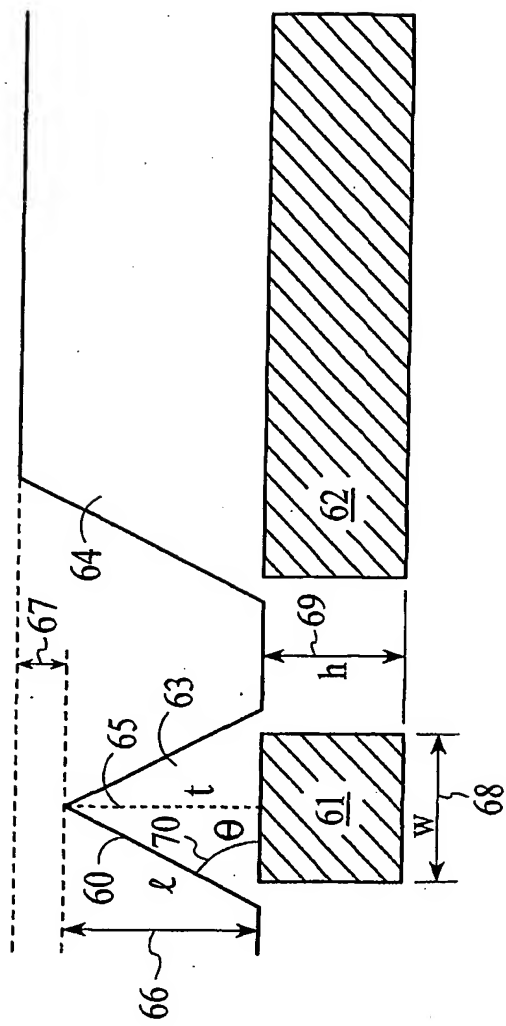
FIG. 1
(PRIOR ART)

FIG. 2
(PRIOR ART)

FIG. 3

FIG. 4

FIG. 5

FIG. 7

FIG. 6B

FIG. 6A